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S11	10	703/20.ccls. and @PD>"20080701"	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2008/11/04 13:23
S12	236	soc and verif\$7 and ((test adj bench) or testbench)	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2008/11/04 13:26


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K Albin, M Inc, TX Austin - Design Automation Conference, 2001. Proceedings, 2001 - [ieeexplore.ieee.org](#)  
 ... 3.1.3 **SoC** designs are large and complex, and so is the ... 3.2 Interface Monitors Figure  
 1 shows the basic components of a unit-level **verification testbench**. ...

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[book] [System-On-A-Chip Verification: Methodology and Techniques](#)

P Rashinkar, P Paterson, L Singh - 2001 - [books.google.com](#)

... This anecdote motivates this book on **SOC verification**. Effective **verification**  
 is fundamental to design reuse ... be accompanied by a reusable "complete" **testbench** ...

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[book] [Surviving the Soc Revolution: A Guide to Platform-Based Design](#)

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... required the transition to RTL-based design capture, and **verification** and acceptance  
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[PDF] [► Practical Approaches to SOC Verification](#)

G Mosenoson - Proceedings of DATE User Forum, 2000 - [cecs.uci.edu](#)

... effect they have on the design of the **testbench**. The rest of this paper focuses  
 on showing practical and novel approaches to the **verification** of **SOC** designs. ...

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[Verification of configurable processor cores](#) - [► sigda.org](#) [PDF]

M Puig-Medina, G Ezer, P Konas - Proceedings of the 37th conference on Design automation, 2000 -  
[portal.acm.org](#)

... **TESTBENCH** Emulated System Monitors ... the processor RTL, the **verification** suite, and  
 the system **test-bench**. ... be easily merged into an **SOC verification** environment. ...

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[C-based SoC design flow and EDA tools: an ASIC and system vendorperspective](#)

K Wakabayashi, T Okamoto - Computer-Aided Design of Integrated Circuits and Systems, ..., 2000 -  
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... and semi-formal verifiers, and **test-bench** generators. The **verification** tools are  
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[A framework for object oriented hardware specification, verification, and synthesis -](#)

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 automation, 2001 - [portal.acm.org](#)

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### How VSIA answers the SOC dilemma

M Birnbaum, H Sachs, FM Inc - Computer, 1999 - [ieeexplore.ieee.org](#)

... Functional **test Test bench** ... for soft and hard virtual components, **SOC verification**, and firm virtual component physical models Manufacturing **Test Phase 2** ...

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### [BOOK] Surviving the Soc Revolution: A Guide to Platform-Based Design

H Chang - 1999 - [books.google.com](#)

... RTI.-based design capture, and **verification** and acceptance ... 6 Surviving the **SOC** Revolution productivity.They ... multiple application-specific **Test** architecture None ...

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... done: the state space is way too large to exhaustively **test** it, and ... 5. CONCLUSIONS

The fundamental problem that **SoC** and Core **verification** efforts deal with ...

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... **TESTBENCH** Emulated System Monitors ... Because our **test-bench** is described completely in terms of modules, integrating it into an **SOC verification test-bench** is as ...

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### C-based SoC design flow and EDA tools: an ASIC and system vendorperspective

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... and semi-formal verifiers, and **test-bench** generators. The **verification** tools are tightly integrated with the HLS ... feature into the C-based **SoC** design environment ...

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